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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,114	02/20/2007	Hans Gustat	536-009.026	4412

4955 7590 01/06/2009

WARE FRESSOLA VAN DER SLUYS & ADOLPHSON, LLP
BRADFORD GREEN, BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
01/06/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/577,114	GUSTAT, HANS	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *2,5-7,14-16,24,27-30 and 38-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,8-13,17-23,25,26 and 31-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/24/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 11/577114 Attorney's Docket #: 536-009.026
Filing Date: 2/20/2007; claimed foreign priority to 10/31/2003

Applicant: Gustat

Examiner: Alexander Williams

This application is a 371 of PCT/EP04/12351 filed 10/28/2004.

Applicant's Pre-Amendment/Drawings filed 2/20/07 has been acknowledged.

Applicant's election of Species I, figures 1, 15 and 16 (claims 1, 3, 4, 8-13, 17-23, 25, 26 and 31-37), filed 10/19/2008, has been acknowledged.

This application contains claims 2, 5-7, 14-16, 24, 27-30 and 38-44 drawn to an invention non-elected without traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The disclosure is objected to because of the following informalities: Applicant's cross reference to related application information should be updated.

Appropriate correction is required.

Claims 3, 4, 8-13, 17-23, 25, 26, 31-37 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 3, 4, 8-13, 17-23, 25, 26, 31-37, the phrase "A chip arrangement" should be –The chip arrangement--.

Any of claims 3, 4, 8-13, 17-23, 25, 26, 31-37 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 4, 8-13, 17-23, 25, 26 and 31-37, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Drost et al. (WO # 2004/012265 A1).

1. Drost et al. (figures 1 to 15) specifically figures 2 and 3 show a chip arrangement comprising a first chip which has at least one first signal interface with first coupling elements arranged along a first line in a first number density and at least one second chip which has at least one second signal interface with second coupling elements arranged along a second line in a second number density, in which the first signal interface is provided along an edge of the first chip and the second signal interface is provided along an edge of the second chip, in which the first and second coupling elements are adapted to permit contactless signal transmission between the first and second signal interfaces, in which the first and second chips are so arranged relative to each other that coupling elements of the first and the second signal interfaces can contactlessly transmit signals with each other, wherein said edges of the first and second chips are arranged in mutually facing relationship, in which the longitudinal extent of at least one of the signal interfaces along the line associated therewith is greater than the length of the overlap of the two longitudinal extents, wherein said overlap is the distance which the projection of the first longitudinal extent on to the second longitudinal extent has in common with the second longitudinal extent, and in which one of the signal interfaces has a greater number density of coupling elements than the other **(page 2, lines 22-25; page 3, lines 3-23; and page 14, lines 12-18).**

3. A chip arrangement as set forth in claim 1, Drost et al. show in which the first, second and optionally third and fourth coupling elements are adapted to permit contactless signal transmission by means of electromagnetic, alternatively capacitive, alternatively inductive, alternatively inductive and capacitive coupling between a first and one or more second coupling elements respectively.

4. A chip arrangement as set forth in claim 1, Drost et al. in which the longitudinal extent of that signal interface which has the greater number density is greater.

8. A chip arrangement as set forth in claim 1, Drost et al. in which the number N2 of the coupling elements of the signal interface with the greater number density is in the ratio N2=g*N1+X to the number N1 of the coupling elements of the signal interface with the lesser number density, wherein g is a number greater than 1 and X is the number of the coupling elements which are in the overshoot longitudinal portions of the signal interface or optionally the coupling unit.

9. A chip arrangement as set forth in claim 1, Drost et al. in which the signal interface of that chip which in the signal flow between the first and the second chips forms a receiver and is referred to subsequently as the receiver chip has coupling elements with a greater number density.

10. A chip arrangement as set forth in claim 9, Drost et al. comprises a filter circuit on the receiver chip, which is connected downstream of the signal interface and is adapted to

reconstruct signals sent from coupling elements at the transmitter end on the basis of the signals received by the coupling elements at the receiver end.

11. A chip arrangement as set forth in claim 10, Drost et al. in which the filter circuit has a number of weighting elements which are respectively adapted to multiply signals received by a plurality of coupling elements at the receiver end by variable weighting factors and to add the signals weighted in that way.

12. A chip arrangement as set forth in claim 11, Drost et al. in which coupling elements at the receiver end are connected to a plurality of weighting elements.

13. A chip arrangement as set forth in claim 11, Drost et al. in which the number of the weighting elements is equal to the number of the coupling elements provided at the transmitter end.

17. A chip arrangement as set forth in claim 1, Drost et al. in which the filter circuit additionally or alternatively has a number of filter banks, wherein each filter bank is connected at the input side to a number of coupling elements.

18. A chip arrangement as set forth in claim 17, Drost et al. in which each filter bank has a number of filters and each filter is connected on the input side to a coupling element.

19. A chip arrangement as set forth in claim 18, Drost et al. in which each filter is adapted to deliver an output signal which depends on a weighted sum of the current signal and a

number of signals which preceded it in respect of time at its input.

20. A chip arrangement as set forth in claim 17, Drost et al. in which each filter is adapted to determine its output signal A in accordance with the following formula: A .function. (z) = j = 1 r .times. .times. S .function. (j) w .function. (j , z) wherein S(j) is a signal at a filter input in a time step j, r is the total number of the time steps considered, w is a weighting factor depending on the respective time step j and z is an index identifying the filter.

21. A chip arrangement as set forth in claim 20, Drost et al. in which the filter has a signal delay line with r delay elements, r multipliers and an adder, wherein a multiplier and a delay element are connected in parallel relationship downstream of each except the last delay element, solely a multiplier is connected downstream of the last delay element, and the outputs of the multipliers are connected to parallel inputs of the summing member.

22. A chip arrangement as set forth in claim 18, Drost et al. in which each filter bank has a weighting unit which is adapted to multiply signals received by the filters of the respective filter bank by variable weighting factors and to add the signals weighted in that way.

23. A chip arrangement as set forth in claim 17, Drost et al. comprises a control unit which is connected to the filter banks and which is adapted in a training phase to subject the signals

applied to the coupling elements at the receiver end to correlation with one or more known signal patterns and on the basis of the correlation result to determine the weighting factors of the filters and the weighting circuit.

25. A chip arrangement as set forth in claim 1, Drost et al. in which that chip which forms a transmitter in the signal flow between the first and the second chips has a transmitting circuit which has complementary CMOS transistors.

26. A chip arrangement as set forth in claim 1, Drost et al. in which a chip is a microprocessor and the other chip is a memory chip.

31. A chip for use in an arrangement as set forth in claim 1, Drost et al. show which has at least one first signal interface with first coupling elements arranged along a first line in a first number density or at least one second signal interface with second coupling elements arranged along a second line in a second number density or which has at least one first and at least one second signal interface, and in which the first and optionally the second signal interface is arranged along an edge of the chip.

32. A chip as set forth in claim 31, Drost et al. show in which the first or the second coupling elements are metallic electrically conductive strips arranged in mutually parallel relationship.

33. A chip as set forth in claim 32, Drost et al. show in which the sum of the spacing and the strip width is between 1 and 25 micrometers.

34. A chip as set forth in claim 31, Drost et al. show in which the coupling elements are coils whose magnetic longitudinal axes are arranged in a horizontal plane in parallel relationship with the surface of the chip.

35. A chip as set forth in claim 31, Drost et al. show in which the first coupling elements, alternatively the second coupling elements, alternatively the first and second coupling elements, are covered by an insulating layer.

36. A chip as set forth in claim 31, Drost et al. show having a reference edge for positioning in a chip arrangement.

37. A chip for use in an arrangement as set forth in claim 1, Drost et al. show which has at least one first signal interface with first coupling elements arranged along a first line in a first number density or at least one second signal interface with second coupling elements arranged along a second line in a second number density or which has at least one first and at least one second signal interface, and in which the first and optionally the second signal interface is arranged along an edge of the chip, the chip having the additional features of claim 10.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claims 1, 3, 4, 8-13, 17-23, 25, 26 and 31-37, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Drost et al. (U.S. Patent Application Publication # 2004/0018654 A1) as detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/AOW/
1/6/2009

/Alexander O Williams/
Primary Examiner, Art Unit 2826